

In re Patent Application of:  
**MARIAUD ET AL.**  
Serial No. 09/989,317  
Filing Date: NOVEMBER 20, 2001

**REMARKS**

The Examiner is again thanked for the thorough examination of the present application, and for the courtesies extended to the undersigned attorney during the telephonic interview on June 13, 2006. During the interview, the objections to Claims 5, 11, 17, and 20 were discussed, as were the rejections of Claims 20 and 21 under 35 U.S.C. §112. These claims have been amended as discussed during the interview to overcome the noted objections/rejections. In addition, the rejection of independent Claim 5 based upon the prior art discussed in the background of the present application ("admitted prior art") in view of Lee (U.S. Patent No. 6,256,699) was also discussed. Independent Claims 5, 11, 17, 20 are being amended herein to more clearly define the subject matter thereof over the prior art, as will be discussed further below. No new matter is being added. Claim 22 has been cancelled.

In view of the amendments and the supporting arguments presented in detail below, it is submitted that all of the claims are patentable.

**I. The Claimed Invention**

The present invention is directed to a computer system. As recited in amended independent Claim 5, for example, the computer system includes a master apparatus and a slave apparatus for communicating asynchronously therewith via a universal serial bus (USB) protocol. The slave apparatus includes a sending/receiving circuit for sending and receiving binary

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information to and from the master apparatus and supplying status signals based thereon. Moreover, a plurality of state latches and control circuitry cooperating therewith receive the status signals from the sending/receiving circuit and supply state signals of the sending/receiving circuit based thereon. The slave apparatus further includes a microprocessor for processing applications of the slave apparatus and also for processing the binary information received by the sending/receiving circuit when an interruption signal is supplied. Furthermore, an interruption state latch and a control circuit cooperating therewith supply the interruption signal to the microprocessor once the start of a new message from the master apparatus has been acknowledged and recorded by the sending/receiving circuit. The sending/receiving circuit also acknowledges the start of a following message from the master apparatus while the interrupt signal is supplied.

Independent Claim 11 is directed to a similar computer system, and independent Claim 17 is directed to a related slave apparatus. Independent Claim 20 is directed to a related method.

## II. The Claims Are Patentable

The Examiner rejected independent Claims 5, 11, 17, and 20 over the "admitted prior art" in view of Lee. The admitted prior art describes a typical master-slave computer system arrangement, such as the one illustrated in FIG. 1 of the present application. Beginning on page 2, line 29, it is noted that during different transfer stages between the master apparatus and the slave apparatus, there are provisions which allow the master

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apparatus to repeat its part of the message IN and OUT while the microcontroller (i.e., microprocessor) of the slave apparatus is unavailable. If the phase that follows is a start phase and its microcontroller is unavailable, the slave apparatus returns no signal (no NAK, nor STALL, nor ACK signal), which is interpreted by the master apparatus as a transmission error. In such case the master apparatus resends the message.

Such an operation only appears if the time period during which the slave microcontroller is unavailable exceeds a time interval separating two consecutive messages. However, in high-speed data transfers, these time intervals between two messages are increasingly short. Yet, the microcontroller of the slave apparatus has to perform more and more tasks, while the time periods during which it is unavailable are longer and longer.

At the end of the transfer stages, an interruption of the microcontroller to process the part of the transmitted message may be requested. To this end, a flag CTR is set to the logic 1 state to indicate that an interruption is requested (see FIG. 3(d) of the present application). After a certain time (which depends on the application), the interruption requested by the USB bus is processed. At the end of the interruption, the program executed by the microcontroller returns the flag CTR to the logic 0 state, thus authorizing the transfer of the following part of the message. A software state machine then processes the information concerning the event of the USB message extracted by the interruption routine.

As a result of the above operations, no transfer over

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the USB bus is authorized when the flag is in the logic 1 state. There is, therefore, a dependency between the time for processing an interruption and the time delay in accepting the following transfer, the time for processing the interruption being linked to the microcontroller's operating frequency. Further, the time delay between each transaction depends on the master apparatus in that if that time delay is shorter than the minimum time for processing an interruption by the microcontroller, the following transfer cannot be authorized. This can result in the failure of the transaction.

The Examiner correctly acknowledges that the admitted prior art fails to teach or fairly suggest that the microprocessor processes the binary information received by the sending/receiving circuit when the interruption signal is supplied, that the interruption signal is supplied once the start of a new message has been acknowledged and recorded by the sending/receiving circuit, and that the sending/receiving circuit also acknowledges the start of a following message while the interruption signal is supplied. Nonetheless, the Examiner contends that Lee properly supplies these noted deficiencies.

Lee is directed to a method and apparatus for providing reliable interrupt reception over a buffered bus by utilizing a mailbox register to receive interrupt request information sent after a data write transaction. The data is sent from an initiating peripheral (i.e., slave) device over the buffered bus to arrive with an arbitrary delay at the host (i.e., master device) memory. After completing the sending phase for the data, the initiating peripheral device sends a mailbox register data block containing an interrupt request to a mailbox register

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associated with the host processor. Because the mailbox register data block will necessarily arrive after the receipt of the actual data in the host memory because it is following the actual data through the same buffered bus, the interrupt will be properly sequenced with the receipt of data. See, e.g., col. 2, line 65 through col. 3, line 10 of Lee.

In particular, the Examiner contends that recitation of an interruption signal being supplied once the start of a new message has been acknowledged and recorded by the sending/receiving circuit is met by "acknowledging the completion of transmitting said data by [the] initiating device in Box 74 of FIG. 7" of Lee, and through storage in the target device, i.e., the host memory. Office Action, page 6. Moreover, the Examiner also contends that the recitation of the sending/receiving circuit is provided by the bridge 46 with buffering and host memory, and the acknowledgement of the start of a following message while the interruption signal is provided by the buffering of data sent from the peripheral device to the host in the host memory.

The above-noted independent claims have been amended to recite that the master and slave apparatuses communicate asynchronously via a universal serial bus (USB) protocol, and that the new messages and following message acknowledged by the slave device are from the master apparatus. To the contrary, Lee teaches implementing a synchronized data transfer approach from a peripheral (i.e., slave) device to a host (i.e., master) device. For example, Lee states that "[r]eliability of interrupt reception by a host processor properly synchronized with receipt of data in host memory is accomplished by utilizing a mailbox register to receive

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interrupt request information sent after a data write transaction." Lee, col. 3, lines 40-44 (emphasis added). This is based upon the use of timing signals IRDY and TRDY, which are generated by the bridge 46. See, e.g., col. 4, lines 50-56 of Lee.

Moreover, as the Examiner notes in the Office Action, the acknowledgement of the interruption signal and data buffering operations discussed in Lee are performed by the host, i.e., the master apparatus. In stark contrast, the above-noted independent claims recite that the new and following messages are from the master apparatus, and they are acknowledged by the slave apparatus.

As such, it is respectfully submitted that the prior art fails to teach or fairly suggest all of the recitations of independent Claims 5, 11, 17, and 20 as amended. Their respective dependent claims, which recite yet further distinguishing features, are also patentable over the prior art and require no further discussion herein.

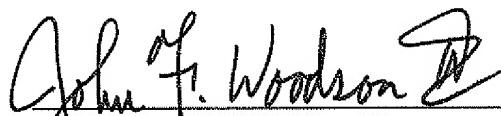
#### CONCLUSIONS

In view of the foregoing, it is submitted that all of the claims are patentable. Accordingly, a Notice of Allowance is respectfully requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

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Respectfully submitted,



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